REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application as amended.

Claims 1-20 are pending in the present application.

The specification is objected to because of informalities.

Claims 13-20 are rejected under 35 U.S.C. §101.

Claims 4, 6, 15, 17 and 19 are objected to because of informalities.

Claims 6 and 17-20 are rejected under 35 U.S.C. §112, first paragraph.

Claims 8 and 16-20 are rejected under 35 U.S.C. §112, second paragraph.

Claims 1-4, 7-8 and 10-16 are rejected under 35 U.S.C. §102(b) as being unpatenable over a publication entitled "Partitioning a Lenient Parallel Language into Sequential Threads" by Sangho Ha, Sangyong Han, and Heunghwan Kim, published in 1995 ("Ha").

Claims 5-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ha in view of U.S. Patent No. 7,768,594 ("Blelloch").

Claim 2 has been canceled.

Claims 1, 4, 6, 8, and 13-20 have been amended.

Paragraphs [0074]-[0077] of the specification have been deleted.

Paragraphs [0032], [0038], [0051], [0057], [0070], [0081], and [0089] of the specification have been amended.

Replacement sheets for Figures 9 and 10 are being submitted herewith.

Support for the amended claims, paragraphs, and replacement sheets of the drawings can be found at paragraphs [0004]-[0091] of the specification, Figures 1-11 in the drawings, and claims 1-20 as originally filed. No new matter has been added.

The specification is objected to because of informalities.

The Office states in part the following.

> In par. [0074] the applicants refer to "the second memory access chain 2->6->12". The examiner does not understand how this memory access chain was derived. Specifically it is noted that no direct dependency exists between nodes 6 and 12 (see e.g. Fig. 8), thus it is believed that the disclosed 'memory access chain ... 6->12' is inconsistent with the rest of the disclosure.

(9/22/2010 Office Action, p. 2).

Applicants have deleted paragraphs [0074]-[0077] of the specification. Replacement sheets for Figures 9 and 10 are submitted herewith. Applicant submits that in view of the amendment to the specification and changes made to the drawings, the objection to the specification has been overcome.

Claims 13-20 are rejected under 35 U.S.C. §101 because the claimed invention was indicated to be directed to non-statutory subject matter.

Claims 13 and 16 have been amended. Claim 13 has been amended to include the limitation "a non-transitory machine accessible medium". Claims 16 has been amended to include the limitation "A code analysis unit implemented on a processor ". Applicants submit that in view of pages 20 and 21 of the "New Interim Patent Subject Matter Eligibility Examination Instructions" issued by the USPTO www.uspto.gov/web/offices/pac/dapp/opla/2009-08-25_interim_101_instructions.pdf, claims 13-20 comply with 35 U.S.C. §101.

Claims 4, 6, 15, 17 and 19 are objected to because of informalities.

Claims 4, 6, 15, 17, and 19 have been amended according to the Office's suggestions.

Applicants submit that in view of the amendments to claims 4, 6, 15, 17, and 19, the objections to the claims have been overcome.

Claims 6 and 17-20 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Specifically, the Office states in part the following.

> Claim 6 recites "if a compute weight of the upstream stage exceeds a predetermined value". While the specification refers repeatedly to a "compute weight" nowhere do the applicants disclose what a "compute weight" is or, more importantly, how it would be calculated. Further, the term "compute weight" does not appear to be a term used in the relevant art. Accordingly those of ordinary skill in the art would not have been enabled to calculate a "compute weight of the upstream stage" in accordance with the applicants disclosed embodiments without undue experimentation.

(9/22/2010 Office Action, pp. 4-5) (Emphasis Added).

Applicants respectfully submit that "weight" is a term used in the relevant art to assess nodes and instructions. Applicants refer the Office, for example, to the following publications. "A Modified State Reduction Algorithm for Computing Weight Enumerators for Convolution Codes" by E.K.S. Au and Wai Ho Mow, published in Information Theory, 2005, ISIT 2005, Proceedings, International Symposium. "Chinese Automatic Summarization Based on Thematic Sentence Discovery" by Meng Wang, Chungui Li, and Xiaorong Wang, published in Fuzzy Systems and Knowledge Discovery, 2007, FSKD 2007, Fourth International Conference. "Hardware Efficient LBIST with Complementary Weights" by Liyang Lai Patel, J.H. Rinderknecht, and T. Wu-Teng Cheng, published in Computer Design: VLSI in Computers and Processors, 2005, ICCD 2005, Proceedings, 2005 IEEE International Conference.

Applicants submit that in view of the explanation above, the rejection of claims 6, and 17-20 under 35 U.S.C. §112, first paragraph have been overcome.

Claims 8 and 16-20 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 8, 17, 18, and 19 have been amended according to the Office's suggestions.

Applicants submit that in view of the amendments, the rejection of claims 8, and 16-20 under 35 U.S.C. §112, second paragraph have been overcome.

Claims 1-20 are rejected under 35 U.S.C. §102(b) and §103(a) as being unpatentable over Ha in view of Blelloch.

It is submitted that Ha and Blelloch do not render claims 1 and 3-20 unpatentable under 35 U.S.C. §102(b) and §103(a).

Ha includes a disclosure of a thread formation scheme to produce efficient sequential threads from programs written in a lenient parallel language. This scheme features graph partitioning based on only long latency instructions, combination of multiple switches and merges introducing a generalized switch and merge, thread merging, and redundant arc elimination using thread precedence relations (see Ha Abstract).

Blelloch includes a disclosure of a method of parallel processing by determining sequential ordering of tasks for processing, assigning priorities to the tasks available on the basis of the sequential ordering, selecting a number of tasks greater than a total number of available parallel processing elements from all available tasks having the highest priorities, partitioning the selected tasks into a number of groups equal to the available number of parallel processing elements, and executing the tasks in the parallel processing elements (see Blelloch Abstract).

Ha and Blelloch do not teach or suggest partitioning instructions in the code among a plurality of processors based on memory access latency associated with the instructions by partitioning memory access dependence chains.

In contrast, Ha discloses partitioning a dataflow Von Neumann RISC hybrid (DAVRID) graph by cutting remote arcs logically. The DAVRID graph is partitioned using dependence set and dominance set, where the dependence set is a variant of Iannucci's dependence set (see Ha Section 4.1). The DAVRID graph is a graph of nodes that includes addition, subtraction, multiplication, comparison, and other arithmetic operations which are not memory access operations (see Ha Figure 3). Clearly, the DAVRID graph is not a memory access dependence chain (see Ha Figure 3). As such, Ha does not teach or suggest partitioning a memory access dependence chain, as claimed.

In contrast, claim 1, as amended states

> A method of compiling code, comprising:
> partitioning instructions in the code among a plurality of processors based on memory access latency associated with the instructions by partitioning memory access dependence chains.

(Claim 1, as Amended) (Emphasis Added).

Claims 15 and 17 include similar limitations. Given that claims 3-12, and 18 depend from claims 1 and 17, it is likewise submitted that claims 3-12, and 18 are also patentable under 35 U.S.C. §102(b) and §103(a) over Ha and Blelloch by virtue of their dependency.

Ha and Blelloch also do note teach or suggest partitioning instructions in code into a plurality of pipeline stages to be executed in parallel by a plurality of processors based on memory access latency associated with the instructions.

In contrast, Ha discloses a thread formation scheme to produce sequential threads from programs written in a lenient parallel language (see Ha Abstract). Thus, not only does Ha not teach or suggest partitioning instructions in code into a plurality of pipeline stages to be executed

in parallel, Ha in fact, by nature of producing sequential threads, teaches away from partitioning instructions in code into a plurality of pipeline stages to be executed in parallel.

Blelloch only discloses methods and means for scheduling parallel processors. Blelloch does not teach or suggest partitioning instructions in code into a plurality of pipeline stages to be executed in parallel by a plurality of processors based on memory access latency associated with the instructions.

In contrast, claim 13 states

> An article of manufacture comprising a non-transitory machine accessible medium including sequences of instructions, the sequences of instructions including instructions which when executed cause the machine to perform:
> partitioning instructions in code into a plurality of pipeline stages to be executed in parallel by a plurality of processors based on memory access latency associated with the instructions.

(Claim 13, as Amended) (Emphasis Added).

Claim 16 includes similar limitations. Given that claims 14-15, and 17-20 depend from claims 13 and 16, it is likewise submitted that claims 14-15, and 17-20 are also patentable under 35 U.S.C. §102(b) and §103(a) over Ha and Blelloch by virtue of their dependency.

Ha and Blelloch also do not teach or suggest partitioning a memory access dependence chain into an upstream stage by assigning a first number of desired upstream nodes to the upstream stage, wherein the number of desired upstream nodes is the length of the memory access dependence chain divided by a pipelining degree.

The Office states in part the following.

> Claim 5: The rejection of claim 4 is incorporated; further Ha does not disclose the number of desired upstream nodes is the length of the memory access dependence chain divided by a pipelining degree.
>
> Blelloch teaches partitioning code such that the number of desired upstream nodes is the length of the memory access dependence chain divided by a pipelining degree (col. 4, lines 19-22 "In step 610, the assignment manager AM1 partitions the

> N selected tasks to p groups of size approx (N/p) each, where p is the number of processing elements PE1").

(9/22/2010 Office Action, p. 10) (Emphasis Added).

Applicants submit that Blelloch discloses partitioning N selected tasks to p groups. However, N is described by Blelloch as being a number of available tasks which have the highest assigned priority, not a number reflecting all available tasks (see Blelloch column 4, lines 13-17). Thus, Blelloch does not teach of suggest a length of the memory access dependence chain divided by a pipelining degree, as claimed.

In contrast, claim 5 states

> The method of Claim 4, wherein the number of desired upstream nodes is the length of the memory access dependence chain divided by a pipelining degree.

(Claim 5) (Emphasis Added).

In view of the arguments set forth herein, it is respectfully submitted that the applicable objections and rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1, and 3-20 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicants' attorney (217-377-2500) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-4238.

Respectfully submitted,
Customer Number: 45512
217-377-2500

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24 day of January, 2011.

/Mary Jacobs/

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